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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

DATE MAILED: 05/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/733,896	KLEIN, DEAN A.	
	Examiner	Art Unit	
	Shawn Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7, 9-13, 15-17, 19-29, 32-40, 42-50 and 52-54* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7, 9-13, 15-17, 19-29, 32-40, 42-50 and 52-54* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/14/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Terminal Disclaimer

1. The terminal disclaimer filed on 14 March 2006 disclaiming the terminal portion of any patent granted on this application which would extend beyond the expiration date of the full statutory term of any patent issuing from U.S. Patent Application No. 10/724,472 has been reviewed and is accepted. The terminal disclaimer has been recorded.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 14 March 2006 was filed after the filing date of the application on 26 November 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Response to Amendment

3. This Office Action is responsive to the amendment filed on 14 March 2006.

Claims 1-7, 9-13, 15-17, 19-29, 32-40, 42-50 and 52-54 are pending. Claims 8, 14, 18, 30, 31, 41 and 51 are cancelled. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 21, 30, 32, 33, 34, 41, 42, 45, 51 and 53 are rejected under 35 U.S.C 102(b) as being unpatentable over Groves [5,222,225] (hereinafter "Groves").

Per claims 21, 34 and 45, Groves teaches a processor (Fig 1) for data string manipulation comprising:

a data cache means (Fig 1, 20 Memory; Col 3, Line 68; Col 4, Line 1) for storing a plurality of cache lines comprising a plurality of bytes of data (Fig 2A);

a string execution means for manipulating the data in the data cache means, the string execution means coupled to said data cache means (Fig 1, 30 Byte Merge, 22 Byte Rotator);

a general execution means for performing arithmetic and logical instructions (ADD, SUB and BRNE instructions indicate execution of arithmetic and logical operations; see Fig. 9A-9D);

a bus interface means coupled to the string execution means and to the general execution means (there must be a bus for communication between the execution

means and data cache means, see Fig 1. Buses 12, 18, 38, 50 and 54; Col. 3, Ln. 50-67 and Col. 4, Ln. 1-28); and

a means for shifting a selected cache line (Fig 1, 22 Byte Rotator) of the plurality of cache lines coupled to the data cache so as to shift a first cache line of the plurality of cache lines a selected number of bytes (Col 6, Lines 3-30).

It is also clear the method of claim 21 is performed by the processors of claims 34 and 45. It should be noted that the string execution means and the general execution means described above anticipate the first execution unit and the second execution unit of claim 21, respectively.

Per claims 30, 41 and 51, Groves further teaches a bus interface unit (Fig 2B, 18A Memory Bus suggests the existence of a bus interface) is coupled to the string execution unit (Fig 2B, 18A Memory Bus and 22A Byte Rotate; Col 6, Lines 5-9).

Per claim 32, it is clear the claim is already substantially disclosed by claims 21 and 45 as described above.

Per claims 33, 42 and 53, Groves further teaches coupling a register to the cache line shifter so as to store data shifted out of the selected cache line by the cache line shifter (Col 6, Lines 3-42; Col 6, Lines 12-30; a rotator stores data shifted out of one end back to the other end).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 7, 8, 9, 11, 17, 19, 20, 24, 25, 36, 37 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Groves, further in view of Pogue [4,920,483] (hereinafter "Pogue").

Per claims 1, 11, 24, 25, 36, 37 and 52, Groves already substantially discloses the claims as described above, and further teaches a memory controller coupled to the string execution unit ("memory circuit", see Col. 2, Ln. 30-43) and a general execution unit coupled to the memory controller (the general execution unit described in claims 21, 34 and 45 must be coupled to the memory controller to access data). Groves does not particularly point out that the shifter is a barrel shifter which shifts an entire first cache line of the plurality of cache lines a selected number of bytes in a single processor cycle. However, Pogue teaches a memory system that includes a barrel shifter for shifting a plurality of bits in a single processor cycle (see Abstract; Paragraphs 962, 1070 and 1072; Claims 3 and 6), whereas shifting multiple bits using a different type of

shifter instead of a barrel shifter would take multiple processor cycles. Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to use a barrel shifter in Groves' cache memory to facilitate shifting of the entire cache line in order to save processing time.

Per claims 7 and 20, Groves further teaches coupling a register to the barrel shifter so as to store data shifted out of the entire cache line by the barrel shifter (Col 6, Lines 3-42; Col 6, Lines 12-30; a rotator stores data shifted out of one end back to the other end).

Per claims 8 and 17, Groves further teaches a bus interface unit (Fig 2B, 18A Memory Bus suggests the existence of a bus interface) is coupled to the barrel shifter (Fig 2B, 18A Memory Bus and 22A Byte Rotate; Col 6, Lines 5-9).

Per claim 9, it is clear the claim is already substantially disclosed by claims 1 and 45 as described above.

Per claim 19, Groves further teaches the memory controller is configured to be alternatively and independently controlled by the string execution unit and the general execution unit (the string operations executed by the string execution unit and the arithmetic operations executed by the general execution unit access the memory separately and independently, see the assembly language instructions in Figs. 9A-9D).

8. Claims 2, 3, 12, 13, 22, 23, 35, 43, 44, 46, 47, 48 and 54 are rejected under 35 U.S.C 103(a) as being unpatentable over Groves and Pogue, in further view of Lee [5,060,143] (hereinafter "Lee").

Per claims 2, 12, 22, 35, 46 and 47, Groves in combination with Pogue already substantially discloses the claims as described above, and further teaches a comparator for data byte comparison (see Fig 1, Byte Comparator 34 and Col. 4, Ln. 5-8). Groves does not specifically teach a plurality of comparators coupled to the data cache so as to compare data in the entire selected first cache line to a test data string in a single processor cycle. However, Lee teaches a data string manipulation processor that includes a plurality of comparators to compare an group of bytes in a data array to a test data string in a single processor cycle (Fig 3, 140 Comparator Array; Col 1, Lines 53-56; a comparison operation determines the propagation delay of a pipeline stage, which in turn determines the length of a clock cycle in a pipelined processor), thereby executing the comparison in one clock cycle, and thereby conserving processing time than having a single byte comparator. Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention to combine Lee's comparators into Groves' cache memory system in order to reduce the processing time of the compare operation.

Per claims 3, 13, 23 and 54, Groves in combination with Pogue and Lee already substantially discloses the claims as described above, and Groves further teaches at

least one subtractor coupled to the data cache (SUB instruction, see Groves, Fig. 9B and 9C). Although the combined references mentioned above do not teach that a plurality of subtractors used to perform the comparison disclosed in claims 2, 12, 22, 35, 46 and 47, it is obvious to know ordinarily skilled in the art at the time of the Applicant's invention that subtractors can be used in place of the comparators to perform comparison, since output bits of the subtractors can be logically ANDed together to produce a binary value to indicate whether the input values of the subtractors match each other or not.

It is also clear claim 54 is already substantially disclosed by claims 21 and 23 as described above.

Per claims 43 and 44, Groves and Pogue already substantially disclose the claim as described above in further view of Lee, and Lee further teaches a decoder coupled to the plurality of comparators so as to identify a portion of the cache line that contains data matching at least a portion of the test data string (Col 8, Lines 1-4; Col 8; Lines 44-54), wherein the decoder is coupled to the string execution unit and is configured to forward a cache address of the matching cache line data to the string execution unit (Col 8, Lines 1-4). It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that this feature is useful in Grove's cache memory to identify the location of the matching data.

Per claim 48, Groves and Pogue, in further view of Lee, already substantially disclose the claim as described above, and further teach that the number of the plurality of comparators is equal to the number of bytes in the selected cache line (Lee: Col 4, Lines 8-11, 4 bytes and 4 comparators; Groves: Fig 2A, one cache line in Memory/Cache is 4 bytes) in order to compare the entire cache line to the data value in one clock cycle (Lee: Col 1, Lines 53-56; a comparison operation determines the propagation delay of a pipeline stage, which in turn determines the length of a clock cycle in a pipelined processor). It would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that this feature can be added to Grove's cache memory to enable comparison of the entire cache line in one clock cycle.

9. Claims 4, 5, 6, 14, 15, 16, 28, 29, 39, 40, 49 and 50 are rejected under 35 U.S.C 103(a) as being unpatentable over Groves and Pogue, in further view of Tran [5,900,012] (hereinafter "Tran").

Per claims 4, 5, 6, 14, 15, 16, 28, 29, 39, 40, 49 and 50, Groves already substantially discloses the claims in further view of Pogue, but does not specifically point out the string execution unit is in association with a memory controller, which is coupled to a main memory that comprises a DRAM circuit. However, Tran teaches a cache system where a cache line is moved from its original location in the cache to first destination cache line (Col 6, Lines 26-39), and the cache data has an associated main memory which comprises a DRAM circuit (Col 1, Liens 36-39), which uses cheaper technology to manufacture than cache memory, and an associated memory controller

(a cache memory and main memory require a memory controller), for larger storage capacity (Col 1, Lines 36-39). Therefore it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves cache memory system could have an associated main memory comprising a DRAM circuit for larger storage capacity than the cache memory at a lower cost.

10. Claims 10, 26, 38 are rejected under 35 U.S.C 103(a) as being unpatentable over Groves and Pogue, in further view of Papworth et al. [5,404,473] (hereinafter "Papworth").

Per claims 10, 26 and 38, Groves already substantially discloses the claim as described above, but does not particularly point that the data cache comprises a Level 1 cache. However, Papworth teaches a processing system that handles string operations which comprises a Level 1 cache, in order to improve processing speed (Col 6, Lines 5-8). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves' cache memory can incorporate a Level 1 cache in order to improve processing speed

11. Claim 27 is rejected under 35 U.S.C 103(a) as being unpatentable over Groves, in further view of Papworth.

Per claim 27, Groves already substantially discloses the claim as described above, but does not particularly point that the data cache comprises a Level 2 cache.

However, Papworth discloses a processing system that handles string operations which comprises a Level 2 cache, in order to increase storage capacity (Col 6, Lines 5-8). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the Applicant's invention that Groves' cache memory can incorporate a Level 2 cache in order to improve storage capacity.

Response to Arguments

12. Applicant's arguments with respect to claims 1-7, 9-13, 15-17, 19-29, 32-40, 42-50 and 52-54 have been considered but are moot in view of the new grounds of rejection. The original allowable subject matter indicated by the Examiner in the previous Office action has been withdrawn upon further consideration. This Office action is not made final as the Examiner introduced new grounds of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shawn X Gu
Patent Examiner
Art Unit 2189

Reginald G. Bragdon
REGINALD G. BRAGDON
PRIMARY EXAMINER

15 May 2006